

☐ L14 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN

## Accession Number

2002:429483 HCAPLUS Full Text

## Document Number

137:14561

## Title

**Metal foil laminated integrated circuit package**

## Author/Inventor

McLellan, Neil; Fan, Chun Ho; Tsang, Kwok Cheung; Lau, Pik Ling

## Patent Assignee/Corporate Source

Asat Ltd., Hong Kong

## Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002068378	A1	20020606	US 2000-730440	20001205 <--
US 6429048	B2	20020806		

## Abstract

The present invention relates generally to packaging for integrated circuit (IC) devices, and in particular to a method of fabricating a **metal foil laminated** package for **ball** grid arrays. A method of fabricating an integrated circuit package for **ball** grid arrays comprises the following steps: **laminating layers** of fiberglass prepreg and **Cu foil** to a **Cu** plate to create a **3-layer laminated carrier**; **patterning** and etching contact pads for input/output and a power/ground ring; applying a **solder** mask and plating up the contact pads and the ring with a wire bondable **metal** surface; forming **window openings** for receiving semiconductor dies; attaching the dies within the **windows**, wire bonding the dies to the contact pads and the ring, encapsulating the dies, attaching **solder balls** to the contact pads to create finished packages and singulating the finished packages into individual packages; and attaching the **Cu** plate portion of each of the individual packages to **Cu** plate heat spreader.

## Concept or Classification

76-14 (Electric Phenomena)

## Supplementary Terms

**metal foil** integrated circuit package

## Controlled or Index Terms

Electronic packaging process

(for a **metal foil laminated** integrated circuit package)

Laser ablation

(for etching of **metal foil laminated** integrated circuit package)

Electric contacts

**Lamination**(for **metal foil laminated** integrated circuit package)

Electronic packages

Integrated circuits

Printed circuit boards

Semiconductor devices

(**metal foil laminated** integrated circuit package)

Glass fibers, uses

RL: TEM (Technical or engineered material use); USES (Uses)

(**metal foil laminated** integrated circuit package containing)

Etching

**Soldering**

(of **metal foil laminated** integrated  
circuit package)

Interconnections, electric

(via; for **metal foil laminated** integrated  
circuit package)

12670-46-1

RL: TEM (Technical or engineered material use); USES (Uses)

(contact pad; **metal foil laminated**  
integrated circuit package containing)

**7440-50-8 , Copper ,** uses

RL: TEM (Technical or engineered material use); USES (Uses)

(**foil ; metal foil laminated**  
integrated circuit package containing)

**National Patent Classification**

438106000

**International Patent Classification**

ICM **H01L021-44**

ICS **H01L021-48 ; H01L021-50**

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## Accession Number

2001:152416 HCAPLUS Full Text

## Document Number

134:187108

## Title

***Processes for manufacturing flexible wiring boards and the resulting flexible wiring boards***

## Author/Inventor

Kurita, Hideyuki; Watanabe, Masanao

## Patent Assignee/Corporate Source

Sony Chemicals Corporation, Japan

## Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
(1) EP 1079676	A3	20030827		
JP 3183653	B2	20010709		
US 6737588	B1	20040518	US 2000-640862	20000818 <--
US 2002189857	A1	20021219	US 2002-230329	20020829
US 6729022	B2	20040504		
US 2003234085	A1	20031225	US 2003-423977	20030428

## Abstract

The present invention aims to connect **metal films** without forming any **opening** in a resin **film**. Against a first resin **film** formed on a first **metal film** are pressed **bumps** on a second **metal film** so that the **bumps** are embedded into the first resin **film**. Either 1 of the first **metal film** or the second **metal film** or both is (are) **patterned** while the **bumps** are in contact with the first **metal film**, and the first resin **film** is heat-treated while the top of the first resin **film** is partially exposed to discharge the solvent or moisture from the exposed zone and cure the first resin **film**. After curing, the **bumps** and the first **metal film** may be ultrasonically bonded to each other. A second resin **film** and a **third metal film** may be further **layered** to form a **multilayer** structure.

## Concept or Classification

76-3 (Electric Phenomena) Section cross-reference(s): 72

## Supplementary Terms

manuf **multilayer** flexible wiring board

## Controlled or Index Terms

Electrodeposition

(copper **film** ; processes for manufacturing flexible wiring boards and resulting flexible wiring boards)

Etching

Imidation

Interconnections (electric)

**Multilayers**

Photolithography

(processes for manufacturing flexible wiring boards and resulting flexible wiring boards)

Polyimides, uses

RL: DEV (Device component use); USES (Uses)

(resin **film** ; processes for manufacturing flexible wiring boards and resulting flexible wiring boards)**7440-50-8** , **Copper** , processes

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(metal **film** ; processes for manufacturing flexible wiring boards and resulting flexible wiring boards)

## International Patent Classification

ICM H05K003-46

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## Accession Number

1984:143662 HCAPLUS Full Text

## Document Number

100:143662

## Title

**Beryllium to metal seals**

## Author/Inventor

Bronnes, Robert L.; Sweet, Richard C.; O'Grady, James D.

## Patent Assignee/Corporate Source

North American Philips Corp., USA

## Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 4431709	A	19840214	US 1982-427057	19820929 <--
CA 1201679	A1	19860311	CA 1983-437319	19830922
JP 59082162	A2	19840512	JP 1983-176527	19830926

## Abstract

The Be surface is **coated** with **3 layers** for reliable bonding to an alloy having a similar coefficient of thermal expansion. The 1st **layer** is a cathodically sputtered **film** (preferably 1000-5000 Å thick) of a refractory **metal** (Ta, Nb, Zr, Hf, Ti, or V). A 2nd **film** 4000-10,000 Å thick of refractory **metals** (especially Mo or W) is applied. The 3rd **film** 4000-10,000 Å thick is a brazeable **metal** (especially **Cu** or Ni). Brazing or **soldering** is then used for the joining. The method is suitable for Be **window foils**. Thus, circular Be **foil** .apprx.250 µ thick was degreased, dried, and **coated** on the edges by cathodic sputtering for successive **layers** of Ti 4500, Mo 8000, and Ni 5000 Å thick. The Be **foil** was then inserted into a cylindrical Kovar frame, and brazed in place with Ag-**Cu** alloy in H atmospheric at .apprx.780°. The resulting seal was suitable for vacuum tightness even when cycled between room temperature and 960°.

## Concept or Classification

56-9 (Nonferrous Metals and Alloys)

## Supplementary Terms

beryllium **foil** brazing **coating** ; **window** x ray beryllium **foil**

## Controlled or Index Terms

## Sputtering

(films by, on beryllium **foil** for brazing)

## X-ray tubes

(windows for, beryllium **foil** **coating** for brazing for)

## Soldering

(brazing, of beryllium **foil** , to alloy holders, multilayer **coatings** for)

## Windows

(x-ray, beryllium **foil** **coating** for brazing for)

7439-98-7, uses and miscellaneous 7440-02-0, uses and miscellaneous

7440-32-6, uses and miscellaneous

RL: USES (Uses)

(film , on beryllium **foil** , sputteredmultilayer **coatings** containing, brazing by)

7440-41-7, uses and miscellaneous

RL: USES (Uses)  
(**foil** , brazing of, **multilayer coatings**  
for)

**National Patent Classification**

428649000

**International Patent Classification**

C23C015-00

☐ **L19 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2004 ACS on STN****Accession Number**1981:75636 HCAPLUS Full Text**Document Number**

94:75636

**Title*****Printed circuits resistant to thermal shock effects*****Author/Inventor**

Paunovic, Milan

**Patent Assignee/Corporate Source**

Kollmorgen Technologies Corp., USA

**Patent Information**

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 3016132	A1	19801030	DE 1980-3016132	19800423
<b>US 4303798</b>	<b>A</b>	<b>19811201</b>	<b>US 1979-34210</b>	<b>19790427 &lt;--</b>
GB 2047974	A	19801203	GB 1980-13065	19800421
JP 55145397	A2	19801112	JP 1980-56112	19800424

**Abstract**

To increase the resistance of the through-hole **metalization** in a printed circuit to the effects of sudden heating, as during **soldering** , a **3-layer metalization** is used, preferably **Cu -Ni-Cu** , in which the thermal expansions of the different **metals** compensate each other.

**Concept or Classification**

76-14 (Electric Phenomena)

**Supplementary Terms**

printed circuit **hole metalization multilayer** ; **copper** nickel **metalization** --  
circuit **hole** ; thermal shock resistance printed circuit; expansion thermal  
printed circuit **metalization**

**Controlled or Index Terms**

Electric circuits

(printed, thermal-shock-resistant **metalization** for through  
**holes** in)

Expansion, Dilation and Elongation

(thermal, of **metal coatings** on through  
**holes** in printed circuits, compensation of)

7440-02-0, uses and miscellaneous **7440-50-8** , uses and  
miscellaneous

RL: USES (Uses)

(printed-circuit through **hole multilayer**  
**metalization** containing, thermal shock-resistant)  
**7440-50-8** , uses and miscellaneous

RL: USES (Uses)

(printed-circuit through **hole multilayer**  
**metalization** containing, thermal shock-resistant)

**International Patent Classification**

H05K003-42

☐ L20 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2004 ACS n STN

## Accession Number

1996:88152 HCAPLUS Full Text

## Document Number

124:161782

## Title

*Processes for manufacturing multilayer TAB*

## Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
RD 373006		19950510		

## Abstract

Several processes are disclosed for making **multilayer** tape automated bonding (TAB) for flexible circuits. These processes are simple compared to present methods and are more economical. The processes allow the fabrication of ground-plane two **metal layer** flexible circuits, screened ground-plane two **metal layer** flexible circuits, double-circuit two **metal layer** flexible circuits, plated ground plane two **metal layer** flexible circuits with through **holes**, three **metal layer** flexible circuits, and very fine-line multiple **metal layer** circuits.

## Concept or Classification

76-3 (Electric Phenomena) Section cross-reference(s): 38, 56, 74

## Supplementary Terms

fabrication **multilayer** TAB flexible circuit; polyimide flexible circuit

## Controlled or Index Terms

Electrodeposition and Electroplating

Etching

**Soldering**

Sputtering

(fabrication processes using **multilayer** TAB for flexible circuits)**Metals**, processes

Polyimides, processes

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(fabrication processes using **multilayer** TAB for flexible circuits)**Coating** process(screen; fabrication processes using **multilayer** TAB for flexible circuits)

Electric circuits

(flexible, fabrication processes using **multilayer** TAB for flexible circuits)

Electric conductors

(pastes, fabrication processes using **multilayer** TAB for flexible circuits)

Resists

(photo-, fabrication processes using **multilayer** TAB for flexible circuits)

Lithography

(photo-, UV, fabrication processes using **multilayer** TAB for flexible circuits)

1310-58-3, Potassium hydroxide, reactions

RL: RCT (Reactant); RACT (Reactant or reagent)

(chrome etchant and photoresist remover; fabrication processes using **multilayer** TAB for flexible circuits)

7722-64-7, Potassium permanganate

RL: RCT (Reactant); RACT (Reactant or reagent)  
(chrome etchant; fabrication processes using **multilayer** TAB  
for flexible circuits)  
7440-47-3, Chromium, processes **7440-50-8 , Copper ,**  
processes  
RL: DEV (Device component use); PEP (Physical, engineering or chemical  
process); PROC (Process); USES (Uses)  
(fabrication processes using **multilayer** TAB for flexible  
circuits)  
1310-73-2, Sodium hydroxide, reactions  
RL: RCT (Reactant); RACT (Reactant or reagent)  
(photoresist remover; fabrication processes using **multilayer**  
TAB for flexible circuits)  
**7440-50-8 , Copper ,** processes  
RL: DEV (Device component use); PEP (Physical, engineering or chemical  
process); PROC (Process); USES (Uses)  
(fabrication processes using **multilayer** TAB for flexible  
circuits)

☐ **L20 ANSWER 7 OF 16 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1993:639843 HCAPLUS Full Text

Document Number

119:239843

Title

**Printed circuit including copper -nickel-copper multilayer electric conductor  
and its manufacture**

Author/Inventor

Ishibashi, Masao; Maniwa, Akira; Hirozawa, Koichi; Okada, Keisuke

Patent Assignee/Corporate Source

Nippon Electric Co, Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05211386	A2	19930820	JP 1992-8887	19920122

Abstract

Claimed are (A) a printed circuit board having, successively deposited a **Cu** bottom **layer**, a Ni interlayer, and a **Cu** top **layer**, on an elec. insulating support optionally on the both sides and on inside wall of a through **hole** and (B) manufacture of the circuit by a process including following successive steps; (1) Ni **coating** on the whole surface of the both sides of a **Cu** -clad **laminate**, (2) selectively **opening** a through **hole** on the **laminate**, (3) **Cu** **coating** on the inside wall of the **hole** and the Ni **layer**, and (4) **patterning** the **Cu** -Ni-**Cu** **layer** or (C) manufacture of the circuit by a process including following successive steps; (1') selectively **opening** a **hole** on a **Cu** -clad **laminate**, (2') **Cu** - **coating** inside the **hole** to form a through **hole**, (3') **patterning** the **Cu** **layer** to form a circuit, (4') Ni **coating** on the inside wall of the through **hole** and the circuit, (5') forming a thick **Cu** **film** by electroless **coating** on the Ni **layer**, and (6') selectively **coating** a **solder** resist. The structure prevents diffusion of Sn to **Cu** **layer** in **soldering**.

Concept or Classification

76-14 (Electric Phenomena) Section cross-reference(s): 56

Supplementary Terms

**copper** clad **laminate** circuit board; nickel **copper** **layered** conductor circuit; **soldering** resistance **copper** circuit board; tin diffusion prevention **copper** circuit

**Controlled or Index Terms**

Electric conductors

(**copper** -nickel-**copper** multilayer, for printed circuits)

**Soldering**

(resistance to, of printed circuit, **copper** -nickel-**copper layered** conductor for)

Electric circuits

(printed, prevention of diffusion of, in **copper** -nickel-**copper layered** conductors for)

7440-50-8 , **Copper** , uses

RL: TEM (Technical or engineered material use); USES (Uses)

(elec. conductor, associated with nickel interlayer, for printed circuit, prevention of tin diffusion during **soldering** in)

7440-02-0, Nickel, uses

RL: TEM (Technical or engineered material use); USES (Uses)

(interlayer **film** , for **copper** elec. conductor, for printed circuit, prevention of tin diffusion during **soldering** in)

7440-31-5, Tin, miscellaneous

RL: PEP (Physical, engineering or chemical process); PROC (Process)

(prevention of diffusion of, in **copper** -nickel-**copper layered** conductor, for printed circuit)

**International Patent Classification**

ICM H05K003-24

ICS H05K001-09; H05K003-18; H05K003-42

FILE 'REGISTRY' ENTERED AT 09:47:09 ON 25 MAY 2004

L1 56875 S CU/MF,ELF AND NC=1

FILE 'HCAPLUS' ENTERED AT 09:47:13 ON 25 MAY 2004

L2 1108745 S L1 OR CU OR COPPER

L3 2722578 S PATTERN? OR METAL?

L4 120135 S BALL# OR BUMP? OR SOLDER?

L5 2866 S BLM OR BALL(W)LIMIT? OR UBM OR UNDERBUMP? OR UNDER(W) BUMP?

L6 1276350 S PLASMA? OR CLEAN#### OR IONIS? OR IONIZ?

L7 758945 S WINDOW? OR ACCESS? OR HOLE? OR OPEN?

L8 QUE THIRD? OR 3 OR TERTIAR? OR THREE?

L9 QUE LAMEL? OR FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID?  
OR LAMIN? OR MULTI(W)LAYER? OR MULTILAYER? OR SHEET? OR LEAF? OR  
FOIL? OR COAT? OR TOPCOAT? OR OVERCOAT? OR VENEER? OR SHEATH? OR  
COVER? OR ENVELOP? OR ENCAS? OR ENWRAP? OR OVERSPREAD? OR LINING? OR  
LINER#

L10 166 S L8 AND L9 AND L2 AND L3 AND (L4 OR L5) AND L7

L11 36 S H01L?/IC AND L10

L12 0 S L11 NOT P/DT NOT PD>20011221

L13 36 S L11 AND P/DT

**L14 6 S L13 AND (WO OR US)/AC(P)AD<20011221**

L15 20 S L13 NOT L14 NOT PD>20011221

L16 48 S L8(3A)L9 AND L10

L17 5 S L16 NOT P/DT NOT PD>20011221

L18 29 S L16 AND P/DT NOT L13

**L19 8 S L18 AND (WO OR US)/AC(P)AD<20011221**

**L20 16 S L18 NOT L19 NOT PD>20011221**